

3A6000

V1.5

3A6000

3A6000

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1.

1 32

2 32 64

SoC 3

64 I/O

3A6000 4 8 FCBGA-1190

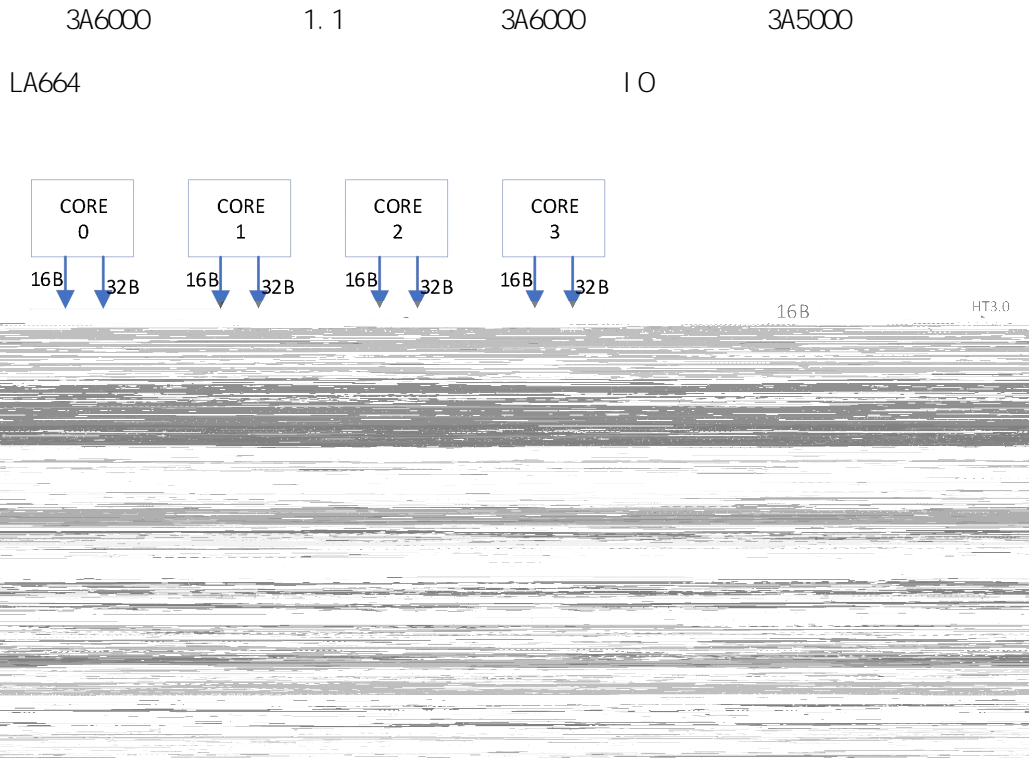
2.0GHz - 2.5GHz

1.1

1.1

	2.0GHz - 2.5GHz
	240GFlops@2.5GHz
	4
	8
	64 LA664 LoongArch® 128/256
	4 4 4
	64KB 64KB 256KB 16MB
	2 72 DDR4-3200 ECC
I/O	1 HyperTransport 3.0 I/O HTO
I/O	1 SPI 1 UART 2 I2C 1 AVS 16 GPIO
	FCBGA1190
	38W@2.5GHz

1.2



1.1

1.3

1190 FCBGA 35mm*35mm

1.4

1 3A6000 HT IO
1.2



1.2

1.5

3A6000

1.2

		*		*		
LS3A6000-HV		1.15V	± 25mV	38W	0 - 70	2.5GHz
LS3A6000-BLL		1.20V	± 25mV	43W	0 - 70	2.5GHz
LS3A6000-LL		1.15V	± 25mV	32W	0 - 70	2.3GHz
LS3A6000M		0.95V	± 25mV	20W	0 - 70	2.0GHz

* VDDN

* VDDN SPEC CPU 2006 RATE

*

1.6

1-2

PMON		
UEFI		
GMAC		
GPIO		
SPI	Serial Peripheral Interface	
WDT	Watchdog Timer	
HDA	High Definition Audio	
I2C	Inter Integrated Circuit	
ROM	Read-Only Memory	
ECC	Error Correcting Code	
PCIe	Peripheral Component Interconnect express	
DDR4		
DI MM	Dual In-line Memory Modules	
UDI MM	Unbuffered Dual In-line Memory Modules	
SODI MM	Small Outline Dual In-line Memory Module	
RDI MM	Registered Dual In-line Memory Modules	
LRDI MM	Load-Reduced Dual In-line Memory Modules	
JTAG		
Loongnix		

1.7

1.7.1

3A6000

3A6000

3A6000

3A6000

1.7.2

LoongArch

1.7.3

1

PMON UEFI

2

Loongnix

1.8

1.8.1

n

n

1.8.2

16 ' hxxx 2 ' bxx 10

DDR_DQ0, DDR_DQ1, ...

DDR_DQ[31: 0]

1.8.3

[] . []

chip_config0_uart_split

0 chip_config0_uart_split

2.

3A6000

1190

-HyperTransport
-DDR4 SDRAM
-
- I/O
-
-JTAG
-
-
-
-GPIO
-SE

2.1

MCO/1_REXT

HT_POWEROK



2.1

2.2

2.1

I	
O	
I/O	
A	

2.3

2.3.1 HyperTransport

3A6000 1 I/O HyperTransport HT

HyperTransport

- 16
- 16
- 2
- 2
- 2
- 2
- 4

HyperTransport

HyperTransport

LDT_STOPn

HT

HT_LDT_STOPn

3A6000

HyperTransport

50KChm

2.2 HT

HT0						
		/				
HT_PowerCK	A5	I/O	HT	PowerCK	VDDE_I/O	
HT_Resetn	A7	I/O	HT	Resetn	VDDE_I/O	
HT_Ldt_Stopn	B7	I/O	HT	Ldt_Stopn	VDDE_I/O	

HT_Ldt_reqn	A6	I/O	HT	Ldt_Reqn	VDDE_I/O
HT_Tx_CADp[15: 0]	C10 A11 C12 A13 C14 A15 C16 A17 G10 E11 G12 E13 G14 E15 G16 E17	O	HT		VDD_HT
HT_Tx_CADn[15: 0]	D10 B11 D12 B13 D14 B15 D16 B17 H10 F11 H12 F13 H14 F15 H16 F17	O	HT		VDD_HT
HT_Tx_CTLp[1: 0]	C8 G8	O	HT		VDD_HT
HT_Tx_CTLn[1: 0]	D8 H8	O	HT		VDD_HT
HT_Tx_CLKp[1: 0]	A9 E9	O	HT		VDD_HT
HT_Tx_CLKn[1: 0]	B9 F9	O	HT		VDD_HT
HT_Rx_CADp[15: 0]	D20 B21 D22 B23	I	HT		VDD_HT

	D24 B25 D26 B27 G20 E21 G22 E23 G24 E25 G26 E27				
HT_Rx_CADn[15: 0]	C20 A21 C22 A23 C24 A25 C26 A27 H20 F21 H22 F23 H24 F25 H26 F27	I	HT	VDD_HT	
HT_Rx_CTLp[1: 0]	D18 G18	I	HT	VDD_HT	
HT_Rx_CTLn[1: 0]	C18 H18	I	HT	VDD_HT	
HT_Rx_CLKp[1: 0]	B19 E19	I	HT	VDD_HT	
HT_Rx_CLKn[1: 0]	A19 F19	I	HT	VDD_HT	
HT_REXT		I	HT	800	VDD_HT

2. 3. 2DDR

3A6000

DDR4 SDRAM

3DS x8 x16

DDR4

■ 72

ECC

■ 9

ECC

10

- 9
 - 15
 - 2 BANK
 - 2 BANK GROUP
 - 4
 - 4
 - 4
 - 4
 - 4 ODT(On Die Termination)
 - 1
 - 1
 - 1
- DDR 2.3 3A6000

2.3 DDR4

		/			
MCO_DQ[63:0]	AB1	I/O		VDDI_Q_DDR	
	AC3				
	AE2				
	AE1				
	AB3				
	AB2				
	AD1				
	AE3				
	AG1				
	AH3				
	AK2				
	AK1				
	AG3				
	AG2				
	AJ1				
	AK3				
	AM				
	AN3				
	AR1				
	AT2				
AN8					
AN2					
AP1					



AR2
AU4
AR5
AT7
AU7
AR4
AT4
AU6
AR7
AR30
AR31
AU33
AT33
AT30
AU30
AR32
AR33
AR35
AT36
AN36
AN37
AU35
AT35
AP37
AN35
AL37
AK35
AH36
AH37
AL35
AL36
AJ37
AH35
AF37
AE35
AC36
AC37
AF35
AF36
AD37
AC35

MOUSE [7: 0]

B

		/			
	AR11 AP11 AT9 AU9 AU11 AT11				
MCO_DCSp[8: 0]	AD2 AJ2 AP2 AT6 AU32 AP36 AJ36 AD36 AP10	I/O	ECC	VDDI_O_DDR	
MCO_DCSn[8: 0]	AD3 AJ3 AP3 AR6 AT32 AP35 AJ35 AD35 AR10	I/O	ECC	VDDI_O_DDR	
MCO_DM[8: 0]	AC1 AH1 AN1 AU5 AU31 AR37 AK37 AE37 AU10	0	DM0-8	VDDI_O_DDR	
MCO_A[13: 0]	AP23 AP18 AT19 AR18 AT18 AN17 AP17 AP16 AT17 AT16	0		VDDI_O_DDR	

		/			
	AR24 AR16 AR15 AT26				
MCO_A17	AU27	O		VDDI_O_DDR	
MCO_BA[1: 0]	AU23 AR23	O	Bank	VDDI_O_DDR	
MCO_BG[1: 0]	AT14 AP15	O	Bank	VDDI_O_DDR	
MCO_VEn	AU24	O	A14	VDDI_O_DDR	
MCO_CASn	AU25	O	A15	VDDI_O_DDR	
MCO_RASn	AT24	O	A16	VDDI_O_DDR	
MCO_SCSn[3: 0]	AP25 AP26 AP24 AT27	O		VDDI_O_DDR	
MCO_CKE[3: 0]	AR14 AU13 AP14 AR13	O		VDDI_O_DDR	
MCO_CKp[3: 0]	AT20 AR19 AP22 AR21	O		VDDI_O_DDR	
MCO_CKn[3: 0]	AR20 AP19 AR22 AT21	O		VDDI_O_DDR	
MCO_ODT[3: 0]	AT25 AU28 AR26 AR28	O	ODT	VDDI_O_DDR	
MCO_Resetn	AP13	O		VDDI_O_DDR	
MCO_ACTn	AU14	O		VDDI_O_DDR	
MCO_PAR	AT22	O		VDDI_O_DDR	
MCO_ALERTn	AU15	I / O	CRC	VDDI_O_DDR	
MCO_REXT	AP28	A	240	VDDI_O_DDR	
MCI_DQ[63: 0]	T5 U7 V6 W7 T7	I / O		VDDI_O_DDR	

		/			
	T6				
	V7				
	V6				
	AA5				
	AB7				
	AD5				
	AD6				
	AA7				
	AA6				
	AC5				
	AD7				
	AF5				
	AG7				
	AJ5				
	AJ6				
	AF7				
	AF6				
	AH5				
	AJ7				
	AL5				
	AL6				
	AN8				
	AN8				
	AL8				
	AL7				
	AM7				
	AN7				
	AN27				
	AJ27				
	AK29				
	AJ29				
	AK27				
	AL27				
	AN29				
	AL29				
	AN33				
	AN81				
	AK33				
	AK32				
	AN31				
	AN32				
	AL33				
	AK31				

		/			
	AH33 AG31 AE33 AE32 AH31 AH32 AF33 AE31 AC33 AC32 AA31 AA30 AC30 AC31 AA33 AA32				
MC1_CB[7: 0]	AE10 AE9 AH10 AH11 AD10 AD9 AG11 AH9	I/O	ECC	VDDI O_DDR	
MC1_DCSp[8: 0]	V5 AC6 AH6 AN6 AJ28 AL32 AF32 AB30 AG9	I/O	ECC	VDDI O_DDR	
MC1_DCSn[8: 0]	V6 AC7 AH7 AN5 AK28 AL31 AF31 AB31 AG10	I/O	ECC	VDDI O_DDR	
MC1_DM[8: 0]	U5	O	DMD-8	VDDI O_DDR	

		/			
	AB5 AG5 AM5 AN28 AM83 AG33 AB33 AF9				
MC1_A[13: 0]	AL20 AK16 AM7 AL16 AJ15 AL15 AM5 AK14 AJ14 AM3 AN21 AL14 AN13 AK23	0		VDDI O_DDR	
MC1_A17	AJ 24	0		VDDI O_DDR	
MC1_BA[1: 0]	AL21 AN20	0	Bank	VDDI O_DDR	
MC1_BG[1: 0]	AM 2 AJ13	0	Bank	VDDI O_DDR	
MC1_VEn	AL22	0	A14	VDDI O_DDR	
MC1_CASn	AN23	0	A15	VDDI O_DDR	
MC1_RASn	AK21	0	A16	VDDI O_DDR	
MC1_SCSn[3: 0]	AN22 AL24 AJ 22 AN25	0		VDDI O_DDR	
MC1_CKE[3: 0]	AK12 AK11 AM1 AM0	0		VDDI O_DDR	
MC1_CKp[3: 0]	AL18 AK17 AK19 AN19	0		VDDI O_DDR	
MC1_CKn[3: 0]	AK18	0		VDDI O_DDR	

SYSRESETn

SYSRESETn

SYSRESETn

64K SYSCLK

I2C UART AVS

I/O

SPI

Flash

17mA

35mA

2.5 SPI



2.3.5

3A6000 1 NMI n 16 GPIO

NSI HT

GPIO INTO-3

NMI n

50KOhm

2.9

		/			
NMI n	NSI	I		VDDE_I/O	

2.3.6 JTAG

3A6000 JTAG

JTAG

JTAG 50KOhm

2.10 JTAG

		/			
TDI	V2	I	JTAG	VDDE_I/O	
TDO	V3	O	JTAG	VDDE_I/O	
TMS	W1	I	JTAG	VDDE_I/O	
TRSTn	W8	I	JTAG	VDDE_I/O	
TCK	W2	I	JTAG	VDDE_I/O	
TSEL[1:0]	U2 U3	I	JTAG 2 b00: LA664 JTAG 2 b01: JTAG	VDDE_I/O	2 b00

2.3.7

3A6000 2.11 SYSCLK

HT_CLKp/HT_CLKn CHIP_CONF1 G[9:4] 3A6000 Core

DDR SYSCLK CHIP_CONF1 G[4] HT

HT HT_CLKp/HT_CLKn
 SYSCLK CHI_P_CONFIG[8] CHI_P_CONFIG

SYSCLK

TESTCLK

CHI_P_CONFIG

2.11

		/	(MHz)		
SYSCLK	Y1	I	25/100	PLL	VDDE_IO
TESTCLK	U1	I	25		VDDE_IO
HT_CLKp/ HT_CLKn	D28 C28	I	100/200	HT	VDD_HT
CHI_P_CONFIG [9:4]	K3 K2 J2 J3 H1 H2	I	-	Core DDR HT	VDDE_IO

2.12 HT

CHI_P_CONFIG[9]	1' b1 HT		CHI_P_CONFIG[7]	1' b0
CHI_P_CONFIG[8]	1' b0 HT PLL	SYSCLK		1' b1
CHI_P_CONFIG[7]	1' b1 HT PLL			
CHI_P_CONFIG[6]	1' b0 PHY	6.4GHz		1' b0
CHI_P_CONFIG[5]	1' b1 PHY	4.8GHz		
CHI_P_CONFIG[4]	1-	25MHz 0-	100MHz	1' b0

CHI_P_CONFIG[9:4]

6' b010100

BIOS

CHI_P_CONFIG[4]

2.3.8 GPIO

3A6000 16 GPIO

GPIO00 - GPIO15

GPIO

IO

GPI O

GPI O

GPI O

17mA 35mA

2. 13 GPI O

GPI O				
0	GPI O00	M8	SPI_CSn1	VDDE_I O
1	GPI O01	K1	SPI_CSn2	VDDE_I O
2	GPI O02	L2	UART1_RXD	VDDE_I O
3	GPI O03	N3	UART1_TXD	VDDE_I O
4	GPI O04	L1	UART1_RTS	VDDE_I O
5	GPI O05	M2	UART1_CTS	VDDE_I O
6	UART1_	mí		

3.

3.1 HyperTransport

3A6000	HyperTransport	IO	HT
16			

3.1.1

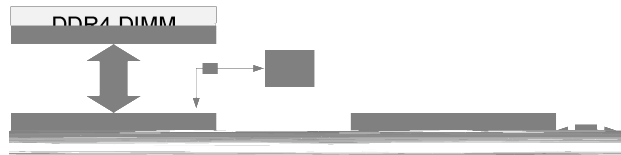
HyperTransport

- HyperTransport 1.03/HyperTransport 3.0
- IO 200 - 3200MHz
- IO Cache

3.1.2

3A6000	HT	IO
--------	----	----

- 3A6000 IO Cache
- IO Cache
- HyperTransport

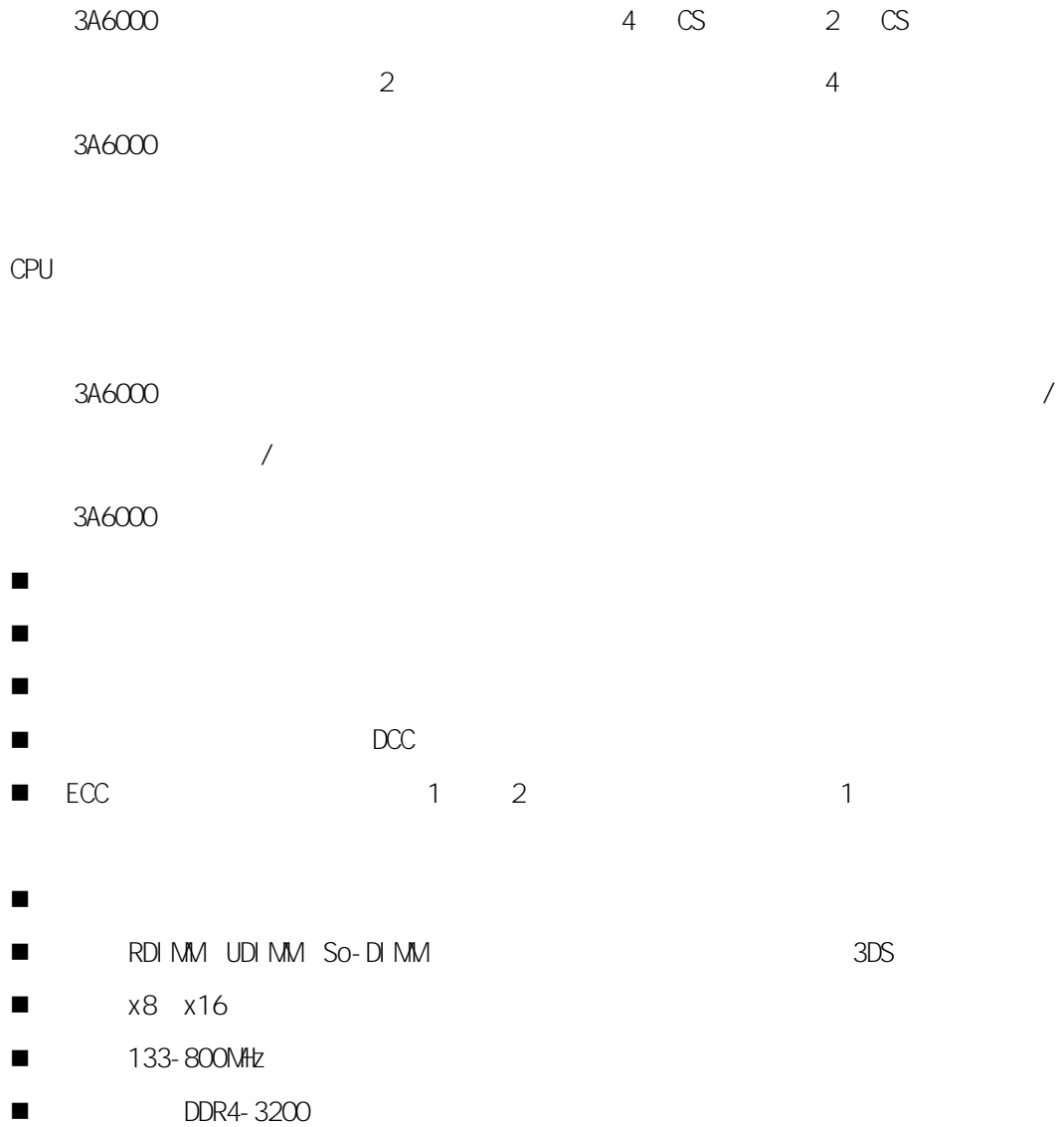


3.1 HT

3.2 DDR

3A6000 DDR4 SDRAM
JESD79-4

3.2.1



3.2.2



- Init_start 0x010 1 Init_start
- DRAM
- (1) Init_start 0x010
- 0
- (2) Init_start 0x010 1
- (3) PHY DLL
- Dll_init_done 0x030 Dll_value_ck 0x030
- Dll_bypass 0x030
- (4) DLL bypass DRAM DRAM
- MRS ZQCL
- (5) Dram_init 0x010

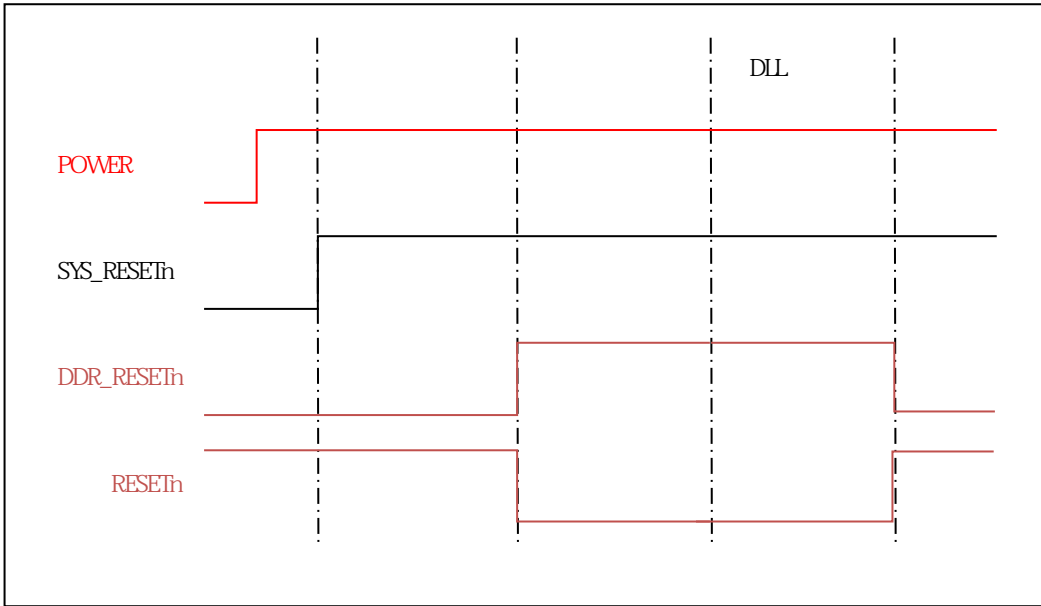
3.2.3

- STR pad_reset_po 0x808
- DDR_RESETEn
- (1) pad_reset_po[1:0] = 2'b00
- DDR_RESETEn

-
-
-
-

3.2

(2) pad_reset_po[1:0]

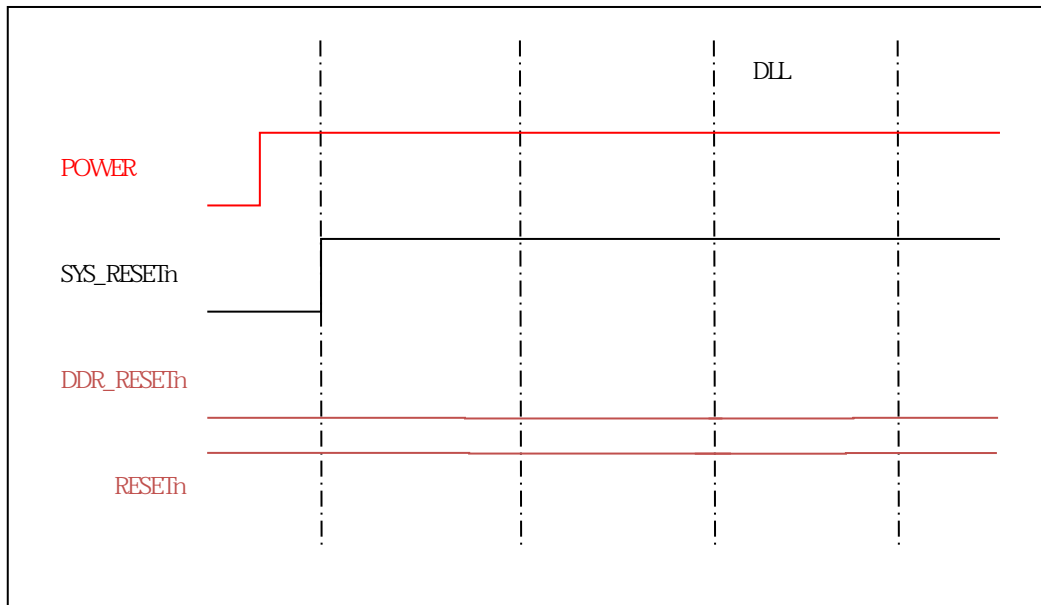


3.3

(3) $pad_reset_po[1:0] = 2'b01$

DDR_RESETh

-



3.4

STR



2

STR

3

4.

4.1

3A6000 SPI Flash

4.2

DOTESTn CHIP_CONFIG

4.1

DOTESTn		
CHIP_CONFIG[9]		HT
CHIP_CONFIG[8]		SYS_CLOCK HT
CHIP_CONFIG[7]		6.4GHz HT PLL VCO
CHIP_CONFIG[6]		
CHIP_CONFIG[5]		
CHIP_CONFIG[4]		100MHz
CHIP_CONFIG[3]		DCDL
CHIP_CONFIG[2]		
CHIP_CONFIG[1]		HT HT1.0
CHIP_CONFIG[0]		SE

5.

5.1

3A6000

SYS_CLOCK

SYSCLK

5.1

Boot Clock	SYS_CLOCK	*1			SPI UART I2C
Main Clock	SYS_PLL	PLL			SYS_PLL Node Clock Core Clock HTcore Clock LA132 Clock Mem Clock Stable Clock
Node Clock	Main Clock	*1			HT
Core0 Clock	Main Clock	*1			0
Core1 Clock	Main Clock	*1			1
Core2 Clock	Main Clock	*1			2
Core3 Clock	Main Clock	*1			3
HTcore Clock	Node Clock	*1			HT 1.25GHz
LA132 Clock	Main Clock	*1			LA132 1GHz
Stable Clock	SYS_CLOCK	*1			
Mem Clock 0/1	MEMPLL0	PLL			0/1
	Main Clock	/2 /4 /8			0/1

5.2

SYSCLK

SYSCLK

100MHz 25MHz

CHIP_CONFIG[4]

HT_CLKp/n

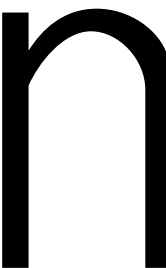
200MHz

5.2

	/	(MHz)		
SYSCLK	I	25/100	PLL Core	VDDE_I/O
HT_CLKp/ HT_CLKn	I	200	HT	VDD_HT

5.2.1

SYSCLK	LVCOM8	1.8v			
V					
V _{ih}			1.25		V
V _{il}				0.4	V
C _{in}				2	pf
Tr			1	2.2	3.6 V/ns
Tf					
Duty Cycle				45% 55%	
Clock jitter		multiple output frequencies switching		74	ps
					b2



*_PLL VDD_HT VDDI_O_DRR VDDE_I/O
3A6000

± 25mV

7.

7.1

7.1

	(° C/W)
	0.726
	0.070
	0.656

LS3A6000-HV/LL/BLL 30KG

LS3A6000M 10KG

7.2 TDP

7.2

TDP Max Power	LS3A6000-HV	80W
TDP Max Power	LS3A6000-BLL	85W
TDP Max Power	LS3A6000-LL	60W
TDP Max Power	LS3A6000M	30W
T_c / T_j		70 ° C / 85 ° C

T_j

7.3

7.3

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6 mm	260 ° C *	260 ° C *	260 ° C *
1.6 mm - 2.5 mm	260 ° C *	250 ° C *	245 ° C *
> 2.5 mm	250 ° C *	245 ° C *	245 ° C *

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature at the rated MSL level

7.4

Profile Feature		Pb-Free Assembly
Average ramp-up rate (Tsm _{ax} to T _p)		3° C/second max.
Preheat	Temperature Min (Tsm _{in})	150 ° C
	Temperature Max (Tsm _{ax})	200 ° C
	Time (Tsm _{in} to Tsm _{ax}) (ts)	60-180 seconds
Time maintained above	Temperature (TL)	217 ° C
	Time (tL)	60-150 seconds
Peak Temperature (T _p)		245° C
Time within 5° C of actual Peak Temperature (tp) ²		20-40 seconds
Ramp-down Rate		6 ° C/second max.
Time 25° C to Peak Temperature		8 minutes max.

8.

I B S

9.

9.1

9.1

VDDN		-0.3	1.35	V
VDDP		-0.3	1.35	V
VDDE_I/O	I/O	-0.3	1.9	V
VDDI_O_DDR	DDR I/O	-0.3	1.26	V
VDD_HT	HT I/O	-0.3	1.3	V
VDD_PHY_DDR	DDRPHY	-0.3	1.35	V
VDD_PLL_DDR	DDR PLL	-0.3	1.4	V
VDD_PLL_SE	SE PLL	-0.3	1.4	V
VDD_PLL_HT	HT PLL	-0.3	1.4	V
VDD_PLL_SYS	SYS PLL	-0.3	1.4	V
VDD_PLL_1V0BU	1V0 Back Up PLL	-0.3	1.4	V
VDD_PLL_1V8BU	1V8 Back Up PLL	-0.3	1.9	V

ESD

ESD HBM 2000V

MSL3

9.2

Absolute storage		-25	100
Sustained storage		-5	40
Relative storage		60%@24	
Tc		0	70

9.2

9.3

VDDN		0.875V	1.20V 1.15V 0.95V M	1.3V	70A 30A

VDDP

0.9V

9.3

9.3.1

VDDN 3 70
 VDDI_O_DDR 3A6000 UDI MM 16GB HT 3.2GHz
 9.5

	ddr	Pvddp	Pvdde_I/O	Pvdd_HT	PPHY_DDR	PPLL_1v25	Pvddi_o_ddr ()
2.55G	3200	<1.0	0.009	1.269	1.375	0.07	5.68
2.55G	3200	<1.0	0.0135	1.299	1.43125	0.0675	5.625
2.55G	3200	<1.0	0.0117	1.245	1.39375	0.06875	5.64

* W

9.3.2



9.1 70

9.3.3

VDDN



9.2.40

9.4

3A6000

Core

I/O

9.5

9.5.1 HyperTransport

HT	HT1.0	HT3.0	200MHz - 3200MHz	DC AC
HT1.0		200 - 800MHz	HT1.03a	
HT3.0		1000 - 3200MHz	HT3.0	

9.5.2 DDR

DDR	DDR4	JESD79-4
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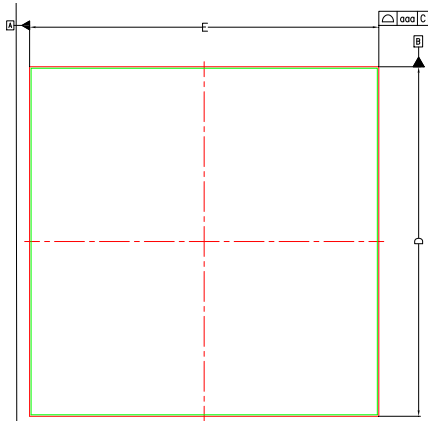
A2	1.142	1.272	1.402
A3	1.260	1.360	1.460
b	0.450	0.550	0.650
D/E	34.900	35.000	35.100
D1/E1		32.9184	
e		0.9144	
g/f		1.0408	
aaa		0.200	
ccc		0.350	
ddd		0.200	
eee		0.250	
fff		0.100	
N		1190	

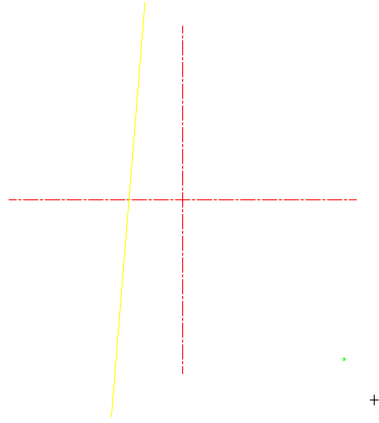
NOTE:

1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M 2009.
3. TERMINAL POSITIONS DESIGNATION PER JE5D 95.

10.1.2 LS3A6000M

3A6000M

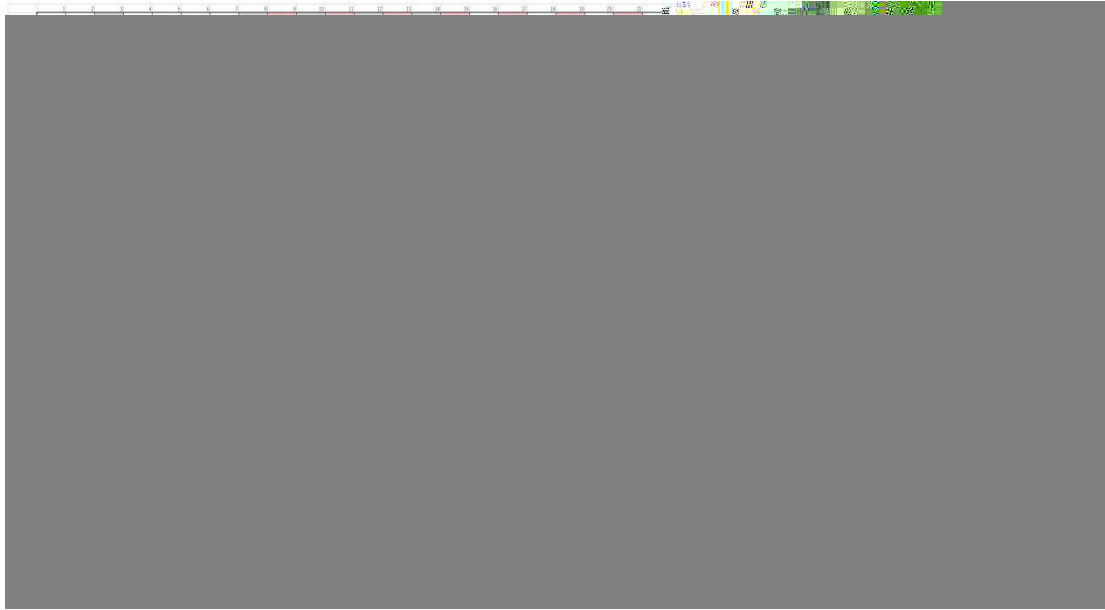




NOTE:

1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M 2009.
3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

10.2



10.3

I/O

HT I/O

VDDP

VDDN

I/O

11.

11.1

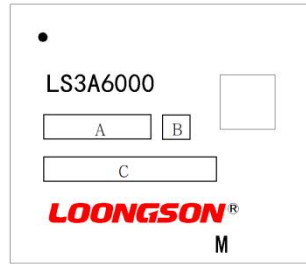
3A6000

LS	3A	6000	-A
			-HV -BLL -LL M

11.2 3A6000 HV/LL/BLL

- 1
- 2 LS3A6000
- 3 Cored By™ LA664
- 4 A
- 5 B
- 6 LOONGSON
- 7 C
- 8

11.3 3A6000M



- 1
- 2 LS3A6000
- 3 A B
- 4
- 5 C
- 6 LOONGSON
- 7 M M

	1	2	3	4	5
A			VSS A3	SE_OSPI_CLK A4	HT_POWERCK A5
B		VSS B2	SE_SPI_CLK B3	SE_I2C_SDA B4	SE_UART0_TX B5
C	VSS C1	SE_RNG0_CLK C2	SE_SPI_CSN C3	SE_I2C_SCL C4	SE_OSPI_I03 C5
D	SE_RNG1_CLK D1	SE_RNG0_CEN D2	SE_SPI_MISO D3	SE_SPI_MOSI D4	SE_OSPI_I00 D5
E	SE_GPI002 E1	SE_GPI000 E2	VDDE_I/O E3	SE_RNG0_DATA E4	VSS E5
F	VSS F1	SE_GPI001 F2	SE_GPI005 F3	SE_RNG1_PE F4	SE_RNG1_CEN F5
G	SE_GPI009 G1	SE_GPI006 G2	SE_GPI008 G3	SE_GPI007 G4	SE_GPI004 G5
H	CHIP_CONF1G8 H1	CHIP_CONF1G9 H2	CHIP_CONF1G3 H3	VDDE_I/O H4	SE_CLK_SEL H5
J	VDDE_I/O J1	CHIP_CONF1G6 J2	CHIP_CONF1G7 J3	CHIP_CONF1G2 J4	SPI_WPN J5
K	GPI001 K1	CHIP_CONF1G5 K2	CHIP_CONF1G4 K3	CHIP_CONF1G1 K4	UART_TXD K5
L	GPI004 L1	GPI002 L2	VSS L3	CHIP_CONF1G0 L4	VSS_PLL_HT L5
M	VDDE_I/O M	GPI005 M2	GPI000 M3	SYSRESETN M4	VSS_PLL_SE M5
N	GPI008 N1	GPI006 N2	GPI003 N3	VDD_PLL_SYS N4	VSS_PLL_SYS N5
P	GPI009 P1	GPI011 P2	GPI007 P3	VSS_PLL_DDR P4	VDD_PLL_DDR P5
R	VSS R1	GPI014 R2	GPI012 R3	VSS R4	VSS R5
T	GPI010 T1	GPI015 T2	GPI013 T3	VSS T4	MC1_D000 T5
U	TESTCLK U1	TSEL0 U2	TSEL1 U3	VSS U4	MC1_DM0N U5
V	DOTESTN V1	TDI V2	TDO V3	VSS V4	MC1_DCS00P V5
W	TM0 W1	TCK W2	TRSTN W3	VSS W4	MC1_D007 W5

Y	SYSCLK Y1	I2C1_SDA Y2	I2C1_SCL Y3	VSS Y4	VSS Y5
AA	VSS AA1	VSS AA2	VSS AA3	VSS AA4	MC1_DC08 AA5
AB	MC0_DC00 AB1	MC0_DC05 AB2	MC0_DC04 AB3	VSS AB4	MC1_DM1N AB5
AC	MC0_DM0N AC1	VSS AC2	MC0_DC01 AC3	VSS AC4	MC1_DC14 AC5
AD	MC0_DC06 AD1	MC0_DCS00P AD2	MC0_DCS00N AD3	VSS AD4	MC1_DC10 AD5
AE	MC0_DC03 AE1	MC0_DC02 AE2	MC0_DC07 AE3	VSS AE4	VSS AE5
AF	VSS AF1	VSS AF2	VSS AF3	VSS AF4	MC1_DC16 AF5
AG	MC0_DC08 AG1	MC0_DC13 AG2	MC0_DC12 AG3	VSS AG4	MC1_DM2N AG5
AH	MC0_DM1N AH1	VSS AH2	MC0_DC09 AH3	VSS AH4	MC1_DC22 AH5
AJ	MC0_DC14 AJ1	MC0_DCS01P AJ2	MC0_DCS01N AJ3	VSS AJ4	MC1_DC18 AJ5
AK	MC0_DC11 AK1	MC0_DC10 AK2	MC0_DC15 AK3	VSS AK4	VSS AK5
AL	VSS AL1	VSS AL2	VSS AL3	VSS AL4	MC1_DC24 AL5
AM	MC0_DC16 AM1	MC0_DC21 AM2	MC0_DC20 AM3	VSS AM4	MC1_DM3N AM5
AN	MC0_DM2N AN1	VSS AN2	MC0_DC17 AN3	VSS AN4	MC1_DCS03N AN5
AP	MC0_DC22 AP1	MC0_DCS02P AP2	MC0_DCS02N AP3	VSS AP4	VSS AP5
AR	MC0_DC18 AR1	MC0_DC23 AR2	VSS AR3	MC0_DC28 AR4	MC0_DC25 AR5
AT	VSS AT1	MC0_DC19 AT2	VSS AT3	MC0_DC29 AT4	VSS AT5
AU		VSS AU2	VSS AU3	MC0_DC24 AU4	MC0_DM3N AU5

	6	7	8	9	10
A	HT_LDT_REQN A6	HT_RSTN A7	VSS A8	HT_TX_CLKOP A9	VSS A10
B	SE_UART0_RX B6	HT_LDT_STOPN B7	VSS B8	HT_TX_CLKON B9	VSS B10
C	SE_CSPI_CSN C6	VSS C7	HT_TX_CTLOP C8	VSS C9	HT_TX_CADOOP C10
D	SE_CSPI_I O1 D6	VSS D7	HT_TX_CTLON D8	VSS D9	HT_TX_CADOON D10
E	SE_RNG0_PE E6	SE_CSPI_I O2 E7	VSS E8	HT_TX_CLK1P E9	VSS E10
F	SE_RNG1_DATA F6	HT_REXT F7	VSS F8	HT_TX_CLK1N F9	VSS F10
G	SE_GPI O03 G6	VSS G7	HT_TX_CTL1P G8	VSS G9	HT_TX_CADO8P G10
H	SPI_SCK H6	VSS H7	HT_TX_CTL1N H8	VSS H9	HT_TX_CADO8N H10
J	SPI_CSN J6	SPI_HOLDN J7	VSS J8	VDD_HT J9	VSS J10
K	UART_RXD K6	SPI_SDO K7	VSS K8	VSS K9	VDD_HT K10
L	VDD_PLL_HT L6	VSS L7	SPI_SDI L8	VSS L9	VDDP L10
M	VDD_PLL_SE M6	VDDE_I O M7	NMIN M8	VSS M9	VDDP M10
N	VSS_PLL_1V8BU N6	VDD_PLL_1V8BU N7	VSS N8	VSS N9	VDDP N10
P	VSS_PLL_1V0BU P6	VDD_PLL_1V0BU P7	VSS P8	VSS P9	VDDP P10
R	VSS R6	VSS R7	VSS R8	VSS R9	VDDP R10
T	MC1_DC05 T6	MC1_DC04 T7	VSS T8	VSS T9	VSS T10
U	VSS U6	MC1_DC01 U7	VSS U8	VSS U9	VDDN U10
V	MC1_DQSOON V6	MC1_DC06 V7	VSS V8	VSS V9	VDDN V10
W	MC1_DC02 W6	MC1_DC03 W7	VSS W8	VSS W9	VSS W10
Y	VSS Y6	VSS Y7	VSS Y8	VSS Y9	VDDN Y10
AA	MC1_DQ13 AA6	MC1_DQ12 AA7	VSS AA8	VSS AA9	VDDN AA10
AB	VSS	MC1_DC09	VSS	VSS	VDDN_SENSE-

	AB6	AB7	AB8	AB9	AB10
AC	MC1_DCS01P AC6	MC1_DCS01N AC7	VSS AC8	VSS AC9	VSS AC10
AD	MC1_DQ11 AD6	MC1_DQ15 AD7	VSS AD8	MC1_CB5 AD9	MC1_CB4 AD10
AE	VSS AE6	VSS AE7	VSS AE8	MC1_CB1 AE9	MC1_CB0 AE10
AF	MC1_DQ21 AF6	MC1_DQ20 AF7	VSS AF8	MC1_DM8N AF9	VSS AF10
AG	VSS AG6	MC1_DQ17 AG7	VSS AG8	MC1_DCS08P AG9	MC1_DCS08N AG10
AH	MC1_DCS02P AH6	MC1_DCS02N AH7	VSS AH8	MC1_CB7 AH9	MC1_CB2 AH10
AJ	MC1_DQ19 AJ6	MC1_DQ23 AJ7	VSS AJ8	VSS AJ9	VSS AJ10
AK	VSS AK6	VSS AK7	VSS AK8	VSS AK9	MC1_REXT AK10
AL	MC1_DQ25 AL6	MC1_DQ29 AL7	MC1_DQ28 AL8	VSS AL9	MC1_RESETN AL10
AM	VSS AM6	MC1_DQ30 AM7	MC1_DQ26 AM8	VSS AM9	MC1_CKE3 AM10
AN	MC1_DCS03P AN6	MC1_DQ31 AN7	MC1_DQ27 AN8	VSS AN9	VSS AN10
AP	VSS AP6	VSS AP7	VSS AP8	MC0_CB1 AP9	MC0_DCS08P AP10
AR	MC0_DCS03N AR6	MC0_DQ31 AR7	VSS AR8	MC0_CB0 AR9	MC0_DCS08N AR10
AT	MC0_DCS03P AT6	MC0_DQ26 AT7	VSS AT8	MC0_CB4 AT9	VSS AT10
AU	MC0_DQ30 AU6	MC0_DQ27 AU7	VSS AU8	MC0_CB5 AU9	MC0_DM8N AU10

	11	12	13	14	15
A	HT_TX_CAD01P A11	VSS A12	HT_TX_CAD03P A13	VSS A14	HT_TX_CAD05P A15
B	HT_TX_CAD01N B11	VSS B12	HT_TX_CAD03N B13	VSS B14	HT_TX_CAD05N B15
C	VSS C11	HT_TX_CAD02P C12	VSS C13	HT_TX_CAD04P C14	VSS C15
D	VSS D11	HT_TX_CAD02N D12	VSS D13	HT_TX_CAD04N D14	VSS D15
E	HT_TX_CAD09P E11	VSS E12	HT_TX_CAD11P E13	VSS E14	HT_TX_CAD13P E15
F	HT_TX_CAD09N F11	VSS F12	HT_TX_CAD11N F13	VSS F14	HT_TX_CAD13N F15
G	VSS G11	HT_TX_CAD10P G12	VSS G13	HT_TX_CAD12P G14	VSS G15
H	VSS H11	HT_TX_CAD10N H12	VSS H13	HT_TX_CAD12N H14	VSS H15
J	VDD_HT J11	VSS J12	VDD_HT J13	VSS J14	VDD_HT J15
K	VSS K11	VDD_HT K12	VSS K13	VDD_HT K14	VSS K15
L	VDDP L11	VDDP L12	VDDP L13	VDDP L14	VDDP L15
M	VDDP M1	VSS M2	VSS M3		
N	VDDP N11	VSS N12	VSS N13		
P	VDDP P11	VDDN P12	VDDN P13		
R	VDDP R11	VDDN R12	VDDN R13		
T	VSS T11	VSS T12	VSS T13		
U	VDDN U11	VDDN U12	VDDN U13		
V	VDDN V11	VDDN V12	VDDN V13		
W	VSS W11	VSS W12	VSS W13		
Y	VDDN Y11	VDDN Y12	VDDN Y13		
AA	VDDN AA11	VDDN AA12	VDDN AA13		
AB	VDDN_SENSE+	VSS	VSS		

	AB11	AB12	AB13		
AC	VSS AC11	VDDN AC12	VDDN AC13		
AD	VSS AD11	VDDN AD12	VDDN AD13		
AE	VSS AE11	VSS AE12	VSS AE13		
AF	VSS AF11	VSS AF12	VSS AF13		
AG	MC1_CB6 AG11	VSS AG12	VDDI_O_DDR AG13	VSS AG14	VDDI_O_DDR AG15
AH	MC1_CB3 AH11	VSS AH12	VSS AH13	VDDI_O_DDR AH14	VSS AH15
AJ	VSS AJ11	VSS AJ12	MC1_BG1 AJ13	MC1_A08 AJ14	MC1_A04 AJ15
AK	MC1_CKE1 AK11	MC1_CKEO AK12	MC1_ALERTN AK13	MC1_A07 AK14	VDDI_O_DDR AK15
AL	VDDI_O_DDR AL11	MC1_ACTN AL12	VDDI_O_DDR AL13	MC1_A11 AL14	MC1_A05 AL15
AM	MC1_CKE2 AM1	MC1_BGO AM2	MC1_A09 AM3	VDDI_O_DDR AM4	MC1_A06 AM5
AN	VSS AN11	VSS AN12	MC1_A12 AN13	VDDI_O_DDR AN14	VDDI_O_DDR AN15
AP	MCO_CB3 AP11	VSS AP12	MCO_RESETN AP13	MCO_CKE2 AP14	MCO_BG1 AP15
AR	MCO_CB2 AR11	VSS AR12	MCO_CKE3 AR13	MCO_CKEO AR14	MCO_A12 AR15
AT	MCO_CB7 AT11	VSS AT12	VDDI_O_DDR AT13	MCO_BGO AT14	VDDI_O_DDR AT15
AU	MCO_CB6 AU11	VSS AU12	MCO_CKE1 AU13	MCO_ACTN AU14	MCO_ALERTN AU15

	16	17	18	19	20
A		HT_TX_CAD07P A17		HT_RX_CLKON A19	
B	VSS B16	HT_TX_CAD07N B17	VSS B18	HT_RX_CLKOP B19	VSS B20
C	HT_TX_CAD06P C16	VSS C17	HT_RX_CTLON C18	VSS C19	HT_RX_CAD00N C20
D	HT_TX_CAD06N D16	VSS D17	HT_RX_CTL0P D18	VSS D19	HT_RX_CAD00P D20
E	VSS E16	HT_TX_CAD15P E17	VSS E18	HT_RX_CLK1P E19	VSS E20
F	VSS F16	HT_TX_CAD15N F17	VSS F18	HT_RX_CLK1N F19	VSS F20
G	HT_TX_CAD14P G16	VSS G17	HT_RX_CTL1P G18	VSS G19	HT_RX_CAD08P G20
H	HT_TX_CAD14N H16	VSS H17	HT_RX_CTL1N H18	VSS H19	HT_RX_CAD08N H20
J	VSS J16	VDD_HT J17	VSS J18	VDD_HT J19	VSS J20
K	VDD_HT K16	VSS K17	VDD_HT K18	VSS K19	VDD_HT K20
L	VDDP L16	VDDP L17	VDDP L18	VDDP L19	VDDP L20
M					
N					
P					
R					
T					
U					
V					
W					
Y					
AA					
AB					
AC					
AD					
AE					
AF					
AG	VSS AG16	VDD_PHY_DDR AG17	VDD_PHY_DDR AG18	VDD_PHY_DDR AG19	VDD_PHY_DDR AG20
AH	VDDI_O_DDR AH16	VSS AH17	VSS AH18	VSS AH19	VSS AH20
AJ	VDDI_O_DDR	MC1_CK1N	VDDI_O_DDR	MC1_CK2N	VDDI_O_DDR

	AJ16	AJ17	AJ18	AJ19	AJ20
AK	MC1_A01 AK16	MC1_CK1P AK17	MC1_CKON AK18	MC1_CK2P AK19	MC1_PAR AK20
AL	MC1_A03 AL16	VDDI_O_DDR AL17	MC1_CKOP AL18	VDDI_O_DDR AL19	MC1_A00 AL20
AM	VDDI_O_DDR AM6	MC1_A02 AM7	VDDI_O_DDR AM8	MC1_CK3N AM9	VDDI_O_DDR AM20
AN	VDDI_O_DDR AN16	MCO_A05 AN17	VDDI_O_DDR AN18	MC1_CK3P AN19	MC1_BA1 AN20
AP	MCO_A07 AP16	MCO_A06 AP17	MCO_A01 AP18	MCO_CK1N AP19	VDDI_O_DDR AP20
AR	MCO_A11 AR16	VDDI_O_DDR AR17	MCO_A03 AR18	MCO_CK1P AR19	MCO_CKON AR20
AT	MCO_A09 AT16	MCO_A08 AT17	MCO_A04 AT18	MCO_A02 AT19	MCO_CKOP AT20
AU		VDDI_O_DDR AU17		VDDI_O_DDR AU19	

	21	22	23	24	25
A	HT_RX_CAD01N A21		HT_RX_CAD03N A23	VSS A24	HT_RX_CAD05N A25
B	HT_RX_CAD01P B21	VSS B22	HT_RX_CAD03P B23	VSS B24	HT_RX_CAD05P B25
C	VSS C21	HT_RX_CAD02N C22	VSS C23	HT_RX_CAD04N C24	VSS C25
D	VSS D21	HT_RX_CAD02P D22	VSS D23	HT_RX_CAD04P D24	VSS D25
E	HT_RX_CAD09P E21	VSS E22	HT_RX_CAD11P E23	VSS E24	HT_RX_CAD13P E25
F	HT_RX_CAD09N F21	VSS F22	HT_RX_CAD11N F23	VSS F24	HT_RX_CAD13N F25
G	VSS G21	HT_RX_CAD10P G22	VSS G23	HT_RX_CAD12P G24	VSS G25
H	VSS H21	HT_RX_CAD10N H22	VSS H23	HT_RX_CAD12N H24	VSS H25
J	VDD_HT J21	VSS J22	VDD_HT J23	VSS J24	VDD_HT J25
K	VSS K21	VDD_HT K22	VSS K23	VDD_HT K24	VSS K25
L	VDDP L21	VDDP L22	VDDP L23	VDDP L24	VDDP L25
M					VSS M25
N					VSS N25
P					VDDN P25
R					VDDN R25
T					VDDN T25
U					VDDN U25
V					VDDN V25
W					VDDN W25
Y					VDDN Y25
AA					VDDN

					AA25
AB					VDDN AB25
AC					VDDN AC25
AD					VDDN AD25
AE					VSS AE25
AF					VSS AF25
AG	VDD_PHY_DDR AG21	VSS AG22	VDD_PHY_DDR AG23	VSS AG24	VDD_PHY_DDR AG25
AH	VSS AH21	VDDI_O_DDR AH22	VSS AH23	VDDI_O_DDR AH24	VSS AH25
AJ	VDDI_O_DDR AJ21	MC1_SCSN2 AJ22	VDDI_O_DDR AJ23	MC1_A17 AJ24	VDDI_O_DDR AJ25
AK	MC1_RASN AK21	VDDI_O_DDR AK22	MC1_A13 AK23	VDDI_O_DDR AK24	MC1_CDT3 AK25
AL	MC1_BAO AL21	MC1_VEN AL22	MC1_ODT0 AL23	MC1_SCSN1 AL24	MC1_CDT1 AL25
AM	VDDI_O_DDR AM21	MC1_SCSNO AM22	VDDI_O_DDR AM23	MC1_CDT2 AM24	VDDI_O_DDR AM25
AN	MC1_A10 AN21	VDDI_O_DDR AN22	MC1_CASN AN23	VDDI_O_DDR AN24	MC1_SCSN3 AN25
AP	VDDI_O_DDR AP21	MC0_CK2P AP22	MC0_A00 AP23	MC0_SCSN2 AP24	MC0_SCSNO AP25
AR	MC0_CK3P AR21	MC0_CK2N AR22	MC0_BA1 AR23	MC0_A10 AR24	VDDI_O_DDR AR25
AT	MC0_CK3N AT21	MC0_PAR AT22	VDDI_O_DDR AT23	MC0_RASN AT24	MC0_CDT0 AT25
AU	VDDI_O_DDR AU21		MC0_BAO AU23	MC0_VEN AU24	MC0_CASN AU25

	26	27	28	29	30
A	VSS A26	HT_RX_CAD07N A27	VSS A28	VDDP A29	VDDP A30
B	VSS B26	HT_RX_CAD07P B27	VSS B28	VDDP B29	VDDP B30
C	HT_RX_CAD06N C26	VSS C27	HT_CLKN C28	VSS C29	VDDP C30
D	HT_RX_CAD06P D26	VSS D27	HT_CLKP D28	VSS D29	VDDP D30
E	VSS E26	HT_RX_CAD15P E27	VSS E28	VDDP E29	VDDP E30
F	VSS F26	HT_RX_CAD15N F27	VSS F28	VDDP F29	VDDP F30
G	HT_RX_CAD14P G26	VSS G27	VSS G28	VDDP G29	VDDP G30
H	HT_RX_CAD14N H26	VSS H27	VSS H28	VDDP H29	VDDP H30
J	VSS J26	VDDP J27	VDDP J28	VDDP J29	VDDP J30
K	VDDP K26	VDDP K27	VSS K28	VDDP K29	VSS K30
L	VDDP L26	VDDP L27	VDDP L28	VSS L29	VDDN L30
M	VSS M26	VDDP M27	VSS M28	VDDN M29	VDDN M30
N	VSS N26	VSS N27	VDDN N28	VDDN N29	VDDN N30
P	VDDN P26	VDDN P27	VDDN P28	VDDN P29	VSS P30
R	VDDN R26	VDDN R27	VDDN R28	VDDN R29	VDDN R30
T	VDDN T26	VDDN T27	VDDN T28	VDDN T29	VDDN T30
U	VDDN U26	VSS U27	VSS U28	VSS U29	VSS U30
V	VDDN V26	VDDN V27	VDDN V28	VDDN V29	VDDN V30
W	VDDN W26	VDDN W27	VDDN W28	VDDN W29	VDDN W30
Y	VDDN Y26	VDDN Y27	VDDN Y28	VSS Y29	VSS Y30
AA	VDDN AA26	VDDN AA27	VSS AA28	VSS AA29	MC1_DC59 AA30
AB	VDDN	VSS	VSS	VSS	MC1_DCS07P

	AB26	AB27	AB28	AB29	AB30
AC	VDDN	VSS	VSS	VSS	MC1_DQ60
	AC26	AC27	AC28	AC29	AC30
AD	VDDN	VSS	VSS	VSS	VSS
	AD26	AD27	AD28	AD29	AD30
AE	VSS	VSS	VSS	VSS	VSS
	AE26	AE27	AE28	AE29	AE30
AF	VSS	VSS	VDD_PHY_DDR	VSS	VSS
	AF26	AF27	AF28	AF29	AF30
AG	VSS	VDD_PHY_DDR	VDD_PHY_DDR	VDD_PHY_DDR	VSS
	AG26	AG27	AG28	AG29	AG30
AH	VSS	VSS	VSS	VSS	VSS
	AH26	AH27	AH28	AH29	AH30
AJ	VSS	MC1_DQ33	MC1_DQS04P	MC1_DQ35	VSS
	AJ26	AJ27	AJ28	AJ29	AJ30
AK	VSS	MC1_DQ36	MC1_DQS04N	MC1_DQ34	VSS
	AK26	AK27	AK28	AK29	AK30
AL	VSS	MC1_DQ37	VSS	MC1_DQ39	VSS
	AL26	AL27	AL28	AL29	AL30
AM	VSS	MC1_DQ32	MC1_DM4N	MC1_DQ38	VSS
	AM26	AM27	AM28	AM29	AM30
AN	VSS	VSS	VSS	VSS	VSS
	AN26	AN27	AN28	AN29	AN30
AP	MCO_SCSN1	VDDI_O_DDR	MCO_REXT	VSS	VSS
	AP26	AP27	AP28	AP29	AP30
AR	MCO_CDT2	VDDI_O_DDR	MCO_CDT3	VSS	MCO_DQ32
	AR26	AR27	AR28	AR29	AR30
AT	MCO_A13	MCO_SCSN3	VDDI_O_DDR	VSS	MCO_DQ36
	AT26	AT27	AT28	AT29	AT30
AU	VDDI_O_DDR	MCO_A17	MCO_CDT1	VSS	MCO_DQ37
	AU26	AU27	AU28	AU29	AU30

	31	32	33	34	35	36	37
A	VDDP A31	VSS A32	VDDN A33	VDDN A34	VSS A35	VDDN A36	
B	VDDP B31	VSS B32	VDDN B33	VDDN B34	VSS B35	VDDN B36	VDDN B37
C	VDDP C31	VSS C32	VDDN C33	VDDN C34	VSS C35	VDDN C36	VDDN C37
D	VDDP D31	VSS D32	VDDN D33	VDDN D34	VSS D35	VDDN D36	VDDN D37
E	VDDP E31	VSS E32	VDDN E33	VDDN E34	VSS E35	VDDN E36	VDDN E37
F	VDDP F31	VSS F32	VDDN F33	VDDN F34	VDDN F35	VDDN F36	VSS F37
G	VDDP G31	VSS G32	VDDN G33	VDDN G34	VDDN G35	VSS G36	VDDN G37
H	VDDP H31	VSS H32	VDDN H33	VDDN H34	VSS H35	VDDN H36	VDDN H37
J	VSS J31	VDDN J32	VDDN J33	VSS J34	VDDN J35	VDDN J36	VSS J37
K	VDDN K31	VDDN K32	VSS K33	VDDN K34	VDDN K35	VSS K36	VDDN K37
L	VDDN L31	VSS L32	VDDN L33	VDDN L34	VSS L35	VDDN L36	VDDN L37
M	VDDN M81	VDDN M82	VDDN M83	VDDN M84	VDDN M85	VDDN M86	VDDN M87
N	VDDN N31	VDDN N32	VDDN N33	VDDN N34	VDDN N35	VDDN N36	VDDN N37
P	VSS P31	VSS P32	VSS P33	VSS P34	VSS P35	VSS P36	VSS P37
R	VDDN R31	VDDN R32	VDDN R33	VDDN R34	VDDN R35	VDDN R36	VDDN R37
T	VDDN T31	VDDN T32	VDDN T33	VDDN T34	VDDN T35	VDDN T36	VDDN T37
U	VSS U31	VSS U32	VSS U33	VSS U34	VSS U35	VSS U36	VSS U37
V	VDDN V31	VDDN V32	VDDN V33	VDDN V34	VDDN V35	VDDN V36	VDDN V37
W	VDDN W81	VDDN W82	VDDN W83	VDDN W84	VDDN W85	VDDN W86	VDDN W87
Y	VSS Y31	VSS Y32	VSS Y33	VSS Y34	AVS_MDATA Y35	AVS_SDATA Y36	VSS Y37
AA	MC1_DQ58 AA31	MC1_DQ63 AA32	MC1_DQ62 AA33	VSS AA34	I2C0_SDA AA35	I2C0_SCL AA36	AVS_CLK AA37



Net Name	Conductor Length (um)
HT_RX_CAD00N	19725.756
HT_RX_CAD00P	19768.68
HT_RX_CAD01N	19691.224
HT_RX_CAD01P	19734.148
HT_RX_CAD02N	19646.261
HT_RX_CAD02P	19689.185
HT_RX_CAD03N	19724.373
HT_RX_CAD03P	19767.297
HT_RX_CAD04N	19605.848
HT_RX_CAD04P	19648.772
HT_RX_CAD05N	19728.393
HT_RX_CAD05P	19771.317
HT_RX_CAD06N	19656.961
HT_RX_CAD06P	19697.207
HT_RX_CAD07N	19660.344
HT_RX_CAD07P	19703.268
HT_RX_CAD08N	19637.795
HT_RX_CAD08P	19678.673
HT_RX_CAD09N	19640.644
HT_RX_CAD09P	19687.581
HT_RX_CAD10N	19648.569
HT_RX_CAD10P	19670.659
HT_RX_CAD11N	19715.817
HT_RX_CAD11P	19747.313
HT_RX_CAD12N	19686.567
HT_RX_CAD12P	19724.723
HT_RX_CAD13N	19681.477
HT_RX_CAD13P	19722.337
HT_RX_CAD14N	19745.202
HT_RX_CAD14P	19786.482
HT_RX_CAD15N	19712.352
HT_RX_CAD15P	19748.082
HT_RX_CLKON	19645.157
HT_RX_CLKOP	19688.081
HT_RX_CLK1N	19661.218
HT_RX_CLK1P	19708.132
HT_RX_CTLON	19645.468

HT_RX_CTL0P	19693.683
HT_RX_CTL1N	19609.49
HT_RX_CTL1P	19636.557
HT_TX_CAD00N	24841.845
HT_TX_CAD00P	24881.728
HT_TX_CAD01N	24885.068
HT_TX_CAD01P	24930.916
HT_TX_CAD02N	24821.225
HT_TX_CAD02P	24861.108
HT_TX_CAD03N	24807.051
HT_TX_CAD03P	24855.162
HT_TX_CAD04N	24790.656
HT_TX_CAD04P	24830.539
HT_TX_CAD05N	24794.284
HT_TX_CAD05P	24815.279
HT_TX_CAD06N	24806.327
HT_TX_CAD06P	24843.906
HT_TX_CAD07N	24857.139
HT_TX_CAD07P	24902.986
HT_TX_CAD08N	24894.115
HT_TX_CAD08P	24932.341
HT_TX_CAD09N	24878.895
HT_TX_CAD09P	24919.109
HT_TX_CAD10N	24787.507
HT_TX_CAD10P	24819.023
HT_TX_CAD11N	24821.277
HT_TX_CAD11P	24867.166
HT_TX_CAD12N	24814.684
HT_TX_CAD12P	24849.95
HT_TX_CAD13N	24786.215
HT_TX_CAD13P	24812.429
HT_TX_CAD14N	24958.103
HT_TX_CAD14P	24917.2
HT_TX_CAD15N	24792.489
HT_TX_CAD15P	24805.095
HT_TX_CLK0N	24844.085
HT_TX_CLK0P	24871.859
HT_TX_CLK1N	24853.75
HT_TX_CLK1P	24819.405
HT_TX_CTL0N	24794.294
HT_TX_CTL0P	24834.177
HT_TX_CTL1N	24887.652

HT_TX_CTL1P	24848.169
MCO_A00	16677.264
MCO_A01	16711.907
MCO_A02	16709.824
MCO_A03	16723.271
MCO_A04	16714.412
MCO_A05	16701.275
MCO_A06	16739.256
MCO_A07	16751.871
MCO_A08	16749.37
MCO_A09	16735.709
MCO_A10	16709.377
MCO_A11	16732.479
MCO_A12	16728.901
MCO_A13	16735.503
MCO_A17	16735.523
MCO_ACTN	16754.93
MCO_ALERTN	16724.656
MCO_BAO	16755.549
MCO_BA1	16739.634
MCO_BGO	16704.839
MCO_BG1	16736.822
MCO_CASN	16751.741
MCO_CBO	17628.548
MCO_CB1	17661.191
MCO_CB2	17633.791
MCO_CB3	17597.016
MCO_CB4	17597.199
MCO_CB5	17622.1
MCO_CB6	17626.458
MCO_CB7	17580.124
MCO_CKON	16822.905
MCO_CKOP	16823.023
MCO_CK1N	16737.138
MCO_CK1P	16729.792
MCO_CK2N	16823.476
MCO_CK2P	16818.12
MCO_CK3N	16808.18
MCO_CK3P	16805.461
MCO_CKE0	16709.536
MCO_CKE1	16725.297
MCO_CKE2	16668.417

MCO_CKE3	16729.033
MCO_DM0N	13961.953
MCO_DM1N	16950.611
MCO_DM2N	20511.914
MCO_DM3N	20276.562
MCO_DM4N	17950.779
MCO_DM5N	19607.741
MCO_DM6N	17013.839
MCO_DM7N	14286.483
MCO_DM8N	17586.295
MCO_DC00	13970.54
MCO_DC01	13933.533
MCO_DC02	13960.408
MCO_DC03	13961.392
MCO_DC04	13973.737
MCO_DC05	13962.222
MCO_DC06	13960.409
MCO_DC07	14008.071
MCO_DC08	16981.6
MCO_DC09	16958.885
MCO_DC10	16988.822
MCO_DC11	16945.336
MCO_DC12	16941.554
MCO_DC13	16980.148
MCO_DC14	16952.004
MCO_DC15	16960.234
MCO_DC16	20502.042
MCO_DC17	20524.667
MCO_DC18	20512.058
MCO_DC19	20583.795
MCO_DC20	20518.992
MCO_DC21	20516.791
MCO_DC22	20546.088
MCO_DC23	20522.411
MCO_DC24	20283.919
MCO_DC25	20248.695
MCO_DC26	20230.653
MCO_DC27	20263.584
MCO_DC28	20293.638
MCO_DC29	20303.87
MCO_DC30	20285.33
MCO_DC31	20217.949

MCO_DQ32	17848.383
MCO_DQ33	17910.261
MCO_DQ34	17884.473
MCO_DQ35	17933.651
MCO_DQ36	17897.674
MCO_DQ37	17818.992
MCO_DQ38	17897.885
MCO_DQ39	17864.32
MCO_DQ40	19656.583
MCO_DQ41	19648.457
MCO_DQ42	19647.217
MCO_DQ43	19648.733
MCO_DQ44	19626.113
MCO_DQ45	19616.819
MCO_DQ46	19618.068
MCO_DQ47	19620.287
MCO_DQ48	17062.169
MCO_DQ49	17039.177
MCO_DQ50	17005.618
MCO_DQ51	17034.421
MCO_DQ52	17052.462
MCO_DQ53	16970.908
MCO_DQ54	17051.492
MCO_DQ55	17033.951
MCO_DQ56	14241.709
MCO_DQ57	14250.735
MCO_DQ58	14285.628
MCO_DQ59	14277.354
MCO_DQ60	14223.206
MCO_DQ61	14279.796
MCO_DQ62	14244.032
MCO_DQ63	14282.275
MCO_DQS00N	14036.303
MCO_DQS00P	14027.285
MCO_DQS01N	17018.476
MCO_DQS01P	17010.269
MCO_DQS02N	20528.914
MCO_DQS02P	20533.624
MCO_DQS03N	20325.58
MCO_DQS03P	20313.318
MCO_DQS04N	17928.36
MCO_DQS04P	17916.011

MCO_DCS05N	19707.554
MCO_DCS05P	19692.263
MCO_DCS06N	17085.359
MCO_DCS06P	17069.946
MCO_DCS07N	14307.867
MCO_DCS07P	14320.31
MCO_DCS08N	17662.045
MCO_DCS08P	17678.569
MCO_CDT0	16779.723
MCO_CDT1	16725.417
MCO_CDT2	16692.806
MCO_CDT3	16741.558
MCO_PAR	16717.145
MCO_RASN	16711.593
MCO_RESETN	16724.844
MCO_REXT	18012.802
MCO_SCSNO	16706.956
MCO_SCSN1	16717.756
MCO_SCSN2	16758.624
MCO_SCSN3	16737.13
MCO_VEN	16760.033
MC1_A00	13723.71
MC1_A01	13728.098
MC1_A02	13733.475
MC1_A03	13705.028
MC1_A04	13770.212
MC1_A05	13751.524
MC1_A06	13707.747
MC1_A07	13711.292
MC1_A08	13696.278
MC1_A09	13751.337
MC1_A10	13735.636
MC1_A11	13713.071
MC1_A12	13725.43
MC1_A13	13698.418
MC1_A17	13727.151
MC1_ACTN	13764.171
MC1_ALERTN	13707.545
MC1_BAO	13762.663
MC1_BA1	13707.486
MC1_BGO	13724.127
MC1_BG1	13699.707

MC1_CASN	13723.335
MC1_CBO	14190.922
MC1_CB1	14278.193
MC1_CB2	14240.562
MC1_CB3	14268.084
MC1_CB4	14264.42
MC1_CB5	14172.775
MC1_CB6	14311.986
MC1_CB7	14233.866
MC1_CKON	13773.623
MC1_CKOP	13770.37
MC1_CK1N	13682.334
MC1_CK1P	13693.492
MC1_CK2N	13859.656
MC1_CK2P	13846.056
MC1_CK3N	13715.118
MC1_CK3P	13714.068
MC1_CKE0	13704.364
MC1_CKE1	13727.498
MC1_CKE2	13765.487
MC1_CKE3	13703.843
MC1_DM0N	13554.097
MC1_DM1N	12627.514
MC1_DM2N	14397.959
MC1_DM3N	17149.273
MC1_DM4N	13661.824
MC1_DM5N	17649.475
MC1_DM6N	13248.364
MC1_DM7N	10751.418
MC1_DM8N	14174.843
MC1_D000	13525.985
MC1_D001	13385.588
MC1_D002	13409.627
MC1_D003	13370.933
MC1_D004	13415.912
MC1_D005	13375.692
MC1_D006	13370.687
MC1_D007	13436.511
MC1_D008	12618.441
MC1_D009	12590.019
MC1_D010	12639.881
MC1_D011	12609.778

MC1_DQ12	12588.178
MC1_DQ13	12609.183
MC1_DQ14	12622.902
MC1_DQ15	12578.846
MC1_DQ16	14390.617
MC1_DQ17	14347.39
MC1_DQ18	14350.483
MC1_DQ19	14366.286
MC1_DQ20	14379.159
MC1_DQ21	14342.757
MC1_DQ22	14361.89
MC1_DQ23	14415.492
MC1_DQ24	17274.746
MC1_DQ25	17128.96
MC1_DQ26	17137.756
MC1_DQ27	17102.622
MC1_DQ28	17105.439
MC1_DQ29	17121.283
MC1_DQ30	17162.148
MC1_DQ31	17123.17
MC1_DQ32	13638.299
MC1_DQ33	13706.491
MC1_DQ34	13652.612
MC1_DQ35	13690.163
MC1_DQ36	13690.329
MC1_DQ37	13678.737
MC1_DQ38	13644.386
MC1_DQ39	13651.8
MC1_DQ40	17627.268
MC1_DQ41	17614.431
MC1_DQ42	17653.516
MC1_DQ43	17634.924
MC1_DQ44	17620.156
MC1_DQ45	17646.076
MC1_DQ46	17666.941
MC1_DQ47	17625.545
MC1_DQ48	13227.069
MC1_DQ49	13220.177
MC1_DQ50	13255.021
MC1_DQ51	13264.957
MC1_DQ52	13224.889
MC1_DQ53	13219.348

MC1_DC54	13214.811
MC1_DC55	13236.316
MC1_DC56	10702.237
MC1_DC57	10722.43
MC1_DC58	10639.143
MC1_DC59	10663.348
MC1_DC60	10725.416
MC1_DC61	10695.768
MC1_DC62	10798.942
MC1_DC63	10733.163
MC1_DCS00N	13458.453
MC1_DCS00P	13463.686
MC1_DCS01N	12658.765
MC1_DCS01P	12668.897
MC1_DCS02N	14385.39
MC1_DCS02P	14386.706
MC1_DCS03N	17188.66
MC1_DCS03P	17184.631
MC1_DCS04N	13689.048
MC1_DCS04P	13694.444
MC1_DCS05N	17703.794
MC1_DCS05P	17701.343
MC1_DCS06N	13304.486
MC1_DCS06P	13289.17
MC1_DCS07N	10755.771
MC1_DCS07P	10738.397
MC1_DCS08N	14213.403
MC1_DCS08P	14210.808
MC1_CDT0	13742.092
MC1_CDT1	13736.597
MC1_CDT2	13727.341
MC1_CDT3	13684.637
MC1_PAR	13739.691
MC1_RASN	13755.615
MC1_RESETN	13748.24
MC1_REXT	16947.674
MC1_SCSNO	13697.798
MC1_SCSN1	13753.325
MC1_SCSN2	13702.364
MC1_SCSN3	13701.921
MC1_VEN	13709.759

V1.0

V1.1 9.3

V1.2 LL 1.15V

1. 2.3.4 2.3.6
 2. 9.2 VDDP 0.95V VDDN VDDP

V1.3 3. 10.1.2

4. 11.2

5. 11.3 M

1. 1.1" " "

2. 1.5 7.1 7.2 9.2 11.1 11.2 BLL

V1.4

3. 9.1 VDD_PLL_1VOBU

4. 9.2